Abstract of the Disclosure

A data input device of a DDR SDRAM includes a clock pulse generator for receiving an internal clock, which operates in a write mode, and outputting a data-in-strobe signal that is a first control signal, a first data buffer an operation of which is controlled by the data-in-strobe signal and an output line of which corresponds to a first global input/output line of the DDR SDRAM, and a second data buffer an operation of which is controlled by the data-in-strobe signal and an output line of which corresponds to a second global input/output line of the DDR SDRAM. If a second control signal is in a low level, first data is directly applied to the first data buffer to be transferred to the first global input/output line, and second data is directly applied to the second data buffer to be transferred to the second global input/output line. If the second control signal is in a high level, the first data is directly applied to the second data buffer to be transferred to the second global input/output line, and the second data is directly applied to the first data buffer to be transferred to the first global input/output line. The data input device can reduce the time for the write operation by directly applying the write-in-strobe signal, which is enabled in the write mode, to the data buffers, and it can also reduce the layout area.